Remarks

In view of the above amendments and the following remarks, reconsideration of the rejections and further examination are requested.

Claims 2 and 3 have been amended to make a number of editorial revisions thereto. These revisions have been made to place the claims in better U.S. form. None of these amendments have been made to narrow the scope of protection of the claims, or to address issues related to patentability, and therefore, these amendments should not be construed as limiting the scope of equivalents of the claimed features offered by the Doctrine of Equivalents.

Claims 1-4 have been rejected under 35 U.S.C. 102(e) as being unpatentable over Shigeta (US 6,064,356). Claims 1-4 have been rejected under 35 U.S.C. 102(e) as being unpatentable over Mikoshiba (US 6,529,204). These rejections are respectfully traversed for the following reasons.

Claim 1 is patentable over Shigeta and Mikoshiba, since claim 1 recites a false contour correcting apparatus having a double bit change detection circuit for detecting a signal portion in a digital image signal, where a change in graduation between two adjacent pixels is twice a unit of graduation level represented by a digital value; and a signal correction circuit for correcting the signal portion in the digital image signal to reduce a false contour caused by digital signal processing performed on the digital image signal based on the double bit change detection signal. Shigeta and Mikoshiba both fail to disclose or suggest these features as recited in claim 1.

Regarding Shigeta, it discloses a false contour correcting circuit 3 for correcting a false contour of pixel data D in a plasma display system. The circuit 3 includes a high-figure bit change detecting circuit 31, a selector control circuit 36, a delay circuit 32, first, second and third data converting circuits 33-35 and a selector 37. (<u>See</u> column 5, lines 16-21 and Figure 3).

In the rejection, the bit change detecting circuit 31 is relied upon as corresponding to the claimed double bit change detection circuit. The bit change detecting circuit 31 receives the pixel data D (i.e., a light emitting pattern) for detecting a change of the high-figure bit of the data at a next field. The bit change detecting circuit 31 outputs a signal P indicating whether or not the bit has changed, to the selector control circuit 36. (<u>See</u> column 56, lines 15-27). On the other hand, the claimed double bit change detection circuit is for detecting a signal portion in a digital image signal, where a change in graduation between two adjacent pixels is twice a unit of graduation level represented by a digital value. It is apparent that while the bit change detecting

circuit 31 detects the change of the high-figure bit of the data at the next field, there is no disclosure or suggest that the bit change detecting circuit 31 detects a signal portion where a change in graduation between two adjacent pixels is twice a unit of graduation level represented by a digital value. As a result, the bit change detecting circuit 31 does not correspond to the double bit change detection circuit recited in claim 1.

Further, the rejection relies on the combination of the selector control circuit 36, the delay circuit 32, the first, second and third data converting circuits 33-35 and the selector 37 as corresponding to the claimed signal correction circuit. The delay circuit 32 also receives the pixel data D and produces a signal with a delay corresponding to the time required for the bit change detecting circuit 31 to perform the above-mentioned processing. The signal including the pixel data D is then input to the first, second and third converting circuits 33-35 which each convert the pixel data D into an 8-bit luminescence level based on a different converting table. The three different luminescence levels are then input to the selector 37 and the selector control circuit 36 controls the selector 37 to output one of the three luminescence levels based on the signal P to correct a "false contour" caused by the emission of light in a particular sub-field of a field. (See column 6, lines 22-65 and column 2, lines 3-44).

Based on this discussion, it is apparent that the selector control circuit 36, the delay circuit 32, the first, second and third data converting circuits 33-35 and the selector 37 are operable to change the luminescence level based on the detection of the change of the high-figure bit by the bit change detecting circuit 31 to correct for the "false contour" caused by the emission of light in a particular sub-field. On the other hand, the claimed signal correction circuit is for correcting the signal portion in the digital image signal to reduce a false contour caused by digital signal processing performed on the digital image signal based on the double bit change detection signal. It is apparent that the false contour corrected by the change in luminescence in the false contour correcting circuit 3 of Shigeta is not the false control caused by digital signal processing performed on a digital image signal that is corrected by the claimed signal correction circuit. As a result, the combination of the selector control circuit 36, the delay circuit 32, the first, second and third data converting circuits 33-35 and the selector 37 do not correspond to the claimed signal correction circuit.

In order to further explain the differences between the false contour correcting circuit 3 of Shigeta and the present invention, as recited in claim 1, the following discussion is provided referring to Reference Drawings 1 and 2 attached (see Attachment 1).

First, as discussed above, it is important to note that even though the term "false contour" is used in both the present invention and Shigeta, the term has a different meaning in each.

In the present invention, a "false contour" occurs as a result of digital signal processing on a video signal, such as grey level correction in order to increase the contrast of an image. An example of the occurrence of a "false contour" with respect to the present invention will be described with reference to Reference Drawing 1.

Squares illustrated in Reference Drawing 1 represent pixels, and numbers in these squares represent digital values indicative of color or brightness of these pixels. Reference Drawing 1 also illustrates an example where three adjacent pixels initially have digital values of 7, 8 and 9. A predetermined digital processing is then preformed on the video signal containing the three pixels and the digital values of these three pixels become 7, 7 and 9. In this case, the video signal before the digital processing has pixel values that are gradually varied by one bit, while the video signal after the digital processing has adjacent pixel values that vary by two bits (7 to 9). That is, after the digital processing, an image portion that would have been gradually varied in color or brightness becomes varied stepwise in color or brightness. If such a double bit change occurs consecutively on a pixel plane, a contour not in the original image appears on the image after the digital processing. This contour is referred to as a "false contour" in the present invention and the "false contour" occurs based on the relationship between two adjacent pixels.

In contrast, a "false contour" of Shigeta occurs due to a factor that is unique to a plasma display panel (PDP) and is different from the "false contour" described above with respect to the present invention which may occur independent of the type of display device that is used. The meaning of the term "false contour" as used in Shigeta is described with respect to Reference Drawing 2.

Generally speaking, it is difficult in the PDP to control the amount of light of pixels. Therefore, the brightness of the pixels is controlled by adjusting the length of a light emitting time in one frame. Specifically, one frame is divided into a plurality of sub-frames (in Reference Drawing 2, four sub-frames denoted by "1", "2", "4" and "8" are illustrated), and light is emitted by a unit of sub-frame. That is, light emission control is performed such that light is emitted

during a time of one or more sub-frames, while light is not emitted during a time of a remainder of sub-frames. With this technique, the brightness of the entire frame is controlled. Moreover, each frame is divided so that time proportions of the four sub-frames each indicate a power of 2. By way of example, in Reference Drawing 2, the time proportions of the four sub-frames are 1:2:4:8. With this, the brightness of the pixels on the frame can be controlled in 16 steps. For example, when the brightness is 7, light is emitted on sub-frames whose time proportions are "1", "2" and "4", respectively (refer to a first frame of Reference Drawing 2, wherein light is not emitted on hatched sub-frames). Furthermore, when the luminance is 8, light is only emitted on a sub-frame whose time proportion is 8 (refer to a second time frame of Reference Drawing 2). Note that, in general, sub-frames are set so that the one shortest in time comes first.

With the above-mentioned scheme for controlling the brightness of pixels on the PDP, however, a "false contour" as defined in Shigeta may occur due to a factor which is different from that in the present invention. For example, as illustrated in Reference Drawing 2, in a case where a pixel has a brightness of 7 on the first frame and then a brightness of 8 on the second frame, light is not emitted on the four consecutive hatched sub-frames (the sub-frame of "8" on the first frame and the sub-frames of "1", "2" and "4" on the second frame). Consequently, these hatched sub-frames are perceived by the human eye as if pixels having a brightness of 0 are on these sub-frames. If such phenomenon occurs in series on the pixel plane, a contour that should not have existed is visible to the human eye. This contour is called a "false contour" in Shigeta. As such, the "false contour" in Shigeta occurs based on a relationship between two adjacent frames on a single pixel, and not based on a relationship between two adjacent pixels.

As such, the "false contour" of the present invention is different in principle from the "false contour" of Shigeta. Although the present invention and Shigeta appear to have the same object, to reduce and correct a false contour, the term "false contour" has different meanings in the present invention and Shigeta. Therefore, their objects are also different from each other and, in turn, the process for preventing a false contour in the present invention is different from that in Shigeta.

As evident from the above description, the "false contour" in the present invention occurs at a portion where digital values of pixels adjacent to each other are varied by two bits, that is, a double bit, which is a minimum quantization unit. In Reference Drawing 1, a false contour occurs at a portion where the digital pixel value is changed from "7" to "9". Claim 1 recites that

a signal portion where a change in graduation between two adjacent pixels is twice a unit of graduation level represented by a digital value (i.e., a false contour) is detected, and then correction is made to the detected signal portion of the video signal.

In contrast, in Shigeta, a light emitting pattern on a frame is changed in order to reduce the occurrence of a "false contour" which is different from that of the present invention. For the purpose of detecting a pixel whose light emitting pattern should be changed, the high-figure bit change detecting circuit 31 of Shigeta detects the high-figure bit change of digital values of adjacent pixels.

As described above, the double bit change detection circuit of the present invention detects a signal portion where a change in graduation between two adjacent pixels is twice a unit of graduation level represented by a digital value, in order to detect a portion where a false contour occurs. On the other hand, the high-figure bit change detecting circuit 31 of Shigeta detects whether the high-figure bit has been changed, in order to detect a portion of a single pixel, which is different from a portion where a false contour occurs between adjacent pixels as described in the present invention (that is, in order to detect a pixel whose light emitting pattern should be changed). As a result, it is apparent that the high-figure bit change detecting circuit 31 of Shigeta does not correspond to the double bit change detection circuit recited in claim 1. Claim 1 and Shigeta perform different processes in order to detect different things.

Moreover, the "false contour" of the present invention cannot be detected by detecting whether a high-figure bit has been changed as disclosed in Shigeta. That is, with the process performed in Shigeta, the effects of the present invention cannot be achieved. An example of this is described below.

As an example, assume that two adjacent pixels each have a digital value represented by four bits (1-16). Also assume that one pixel (first pixel) has a digital value of "10" in decimal (that is, "1010" in hexadecimal), while the other pixel (second pixel) has a digital value of "12" (that is, "1100" in hexadecimal). As described above, in claim 1, it is detected whether the digital value has been changed by two bits, and therefore, a change between the first pixel and the second pixel is detected. With this, whether or not a "false contour", as defined in the present invention, occurs can be detected. In contrast, in Shigeta, what is detected is whether the high-figure bit (here, the most significant bit) has been changed, that is, whether the high-figure bit has been inverted. Therefore, a change between the first pixel and the second pixel is not

detected in Shigeta, since the high-figure bit is "1" in both the first pixel and second pixel. Therefore, whether or not a "false contour" as defined in the present invention occurs cannot be detected by the high-figure bit change detecting circuit 31 of Shigeta.

Furthermore, in another example, assume that the first pixel has a digital value of "7" (that is, "0111" in hexadecimal) and the second pixel has a digital value of "8" (that is, "1000" in hexadecimal). In this example, in claim 1, a change between the first pixel and the second pixel is not detected. In contrast, in Shigeta, the most significant bit has been inverted, and therefore, such a change between the first pixel and the second pixel is detected. As a result, an irrelevant portion where no "false contour" as defined in the present invention occurs is detected.

As evident from the above examples, detecting a signal portion where a change in graduation between two adjacent pixels is twice a unit of graduation level represented by a digital value and detecting whether the high-figure bit has been changed are completely different. Moreover, in the present invention, the "false contour" as defined in the present invention cannot be prevented by detecting whether the high-figure bit has been changed. Further, based on the discussion, it would not have been obvious to include a signal portion where a change in graduation between two adjacent pixels is twice a unit of graduation level represented by a digital value with the system of Shigeta, since the present invention and Shigeta disclose inventions directed to completely different problems.

As such, the present invention as recited in claim 1 and Shigeta are different from each other in processing and, in turn, the object of the present invention cannot be achieved by the processing of Shigeta. Furthermore, Shigeta does not disclose or suggest the "false contour" as defined in the present invention or a measure for preventing such false contour. Therefore, claim 1 is patentable over Shigeta.

Regarding Mikoshiba, it discloses an apparatus for displaying halftone images on a plasma display panel by dividing each frame of an image into a number of sub-frames and turning on and off the sub-frames to change their intensity levels, and therefore, prevent false contours from occurring. (<u>See</u> abstract; column 24, line 55 – column 25, line 44; and Figures 52 and 53). Based on this discussion in Mikoshiba, it is apparent that the apparatus of Mikoshiba is similar to the false contour correcting circuit 3 of Shigeta, since it corrects the false contour generated when light is emitted in sub-frame units based on a bit number that refers to a sub-frame of a specific light intensity level. As a result, it is apparent that Mikoshiba fails to disclose

or suggest the double bit change detection circuit and the signal correction circuit as recited in claim 1.

As for claim 3, it is patentable over Shigeta and Mikoshiba for reasons similar to those set forth above in support of claim 1. That is, claim 3, like above claim 1, recites detecting a signal portion in a digital image signal, where a change in graduation between two adjacent pixels is twice a unit of graduation level represented by a digital value; and correcting the signal portion in the digital image signal to reduce a false contour caused by a digital signal processing performed on the digital image signal based on the detecting, which features are not disclosed or suggested by the references.

Because of the above-mentioned distinctions, it is believed clear that claims 1-4 are allowable over Shigeta and Mikoshiba. Furthermore, it is submitted that the distinctions are such that a person having ordinary skill in the art at the time of invention would not have been motivated to make any combination of the references of record in such a manner as to result in, or otherwise render obvious, the present invention as recited in claims 1-4. Therefore, it is submitted that claims 1-4 are clearly allowable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. The Examiner is invited to contact the undersigned by telephone if it is felt that there are issues remaining which must be resolved before allowance of the application.

Respectfully submitted,

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